1/15 FIG. 1A

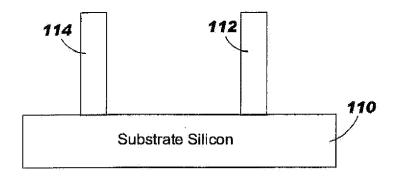
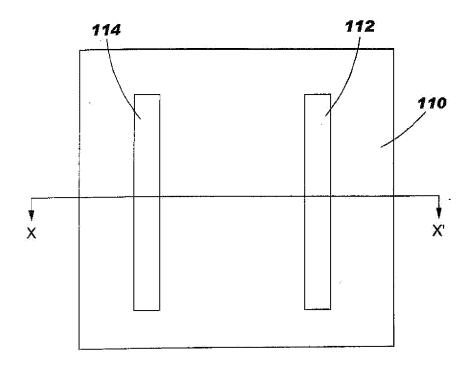


FIG. 1B



2/15 FIG. 2A

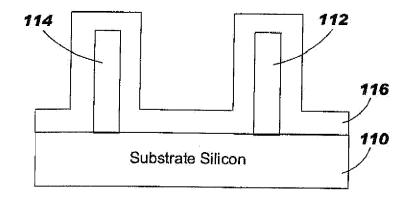
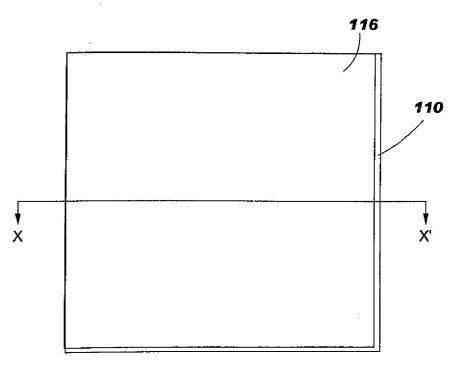


FIG. 2B



3/15 FIG. 3A

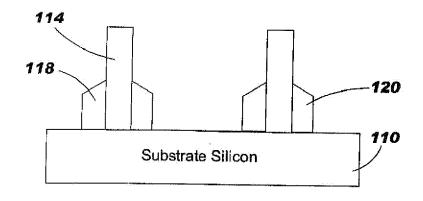
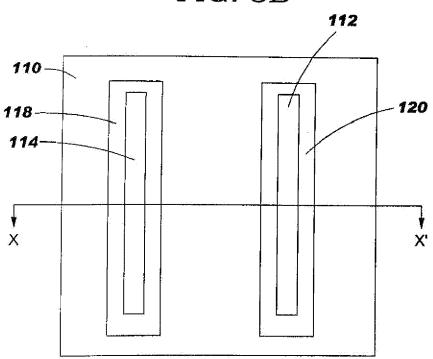


FIG. 3B



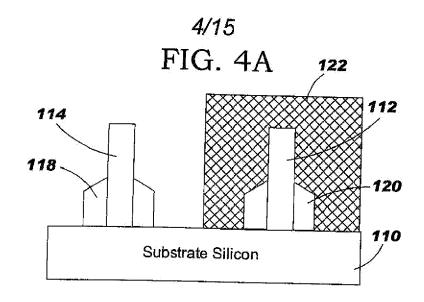
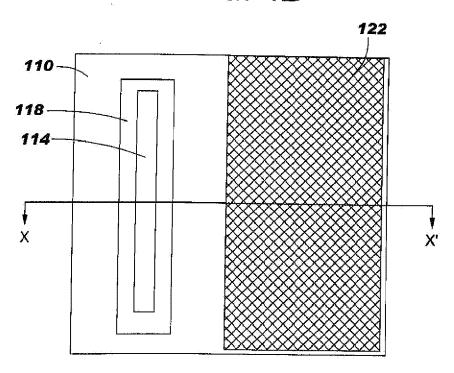


FIG. 4B



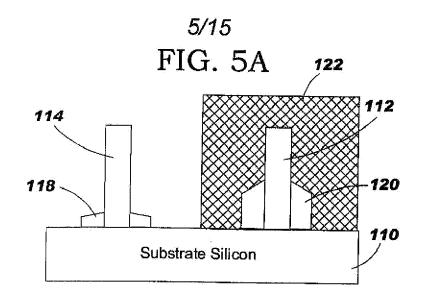
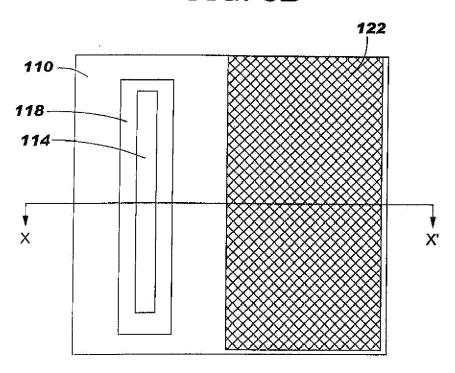


FIG. 5B



6/15 FIG. 6A

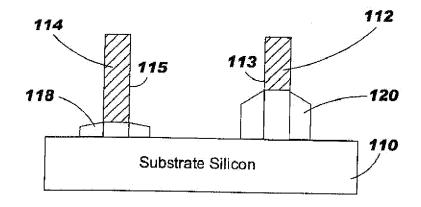
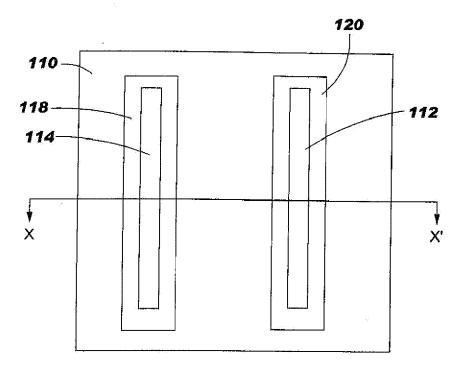
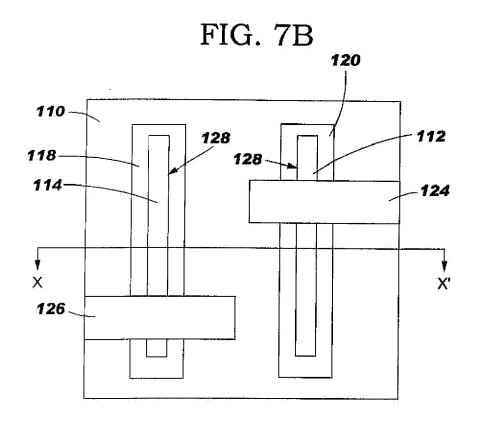


FIG. 6B



7/15
FIG. 7A

126
114
128
128
120
110
Substrate Silicon



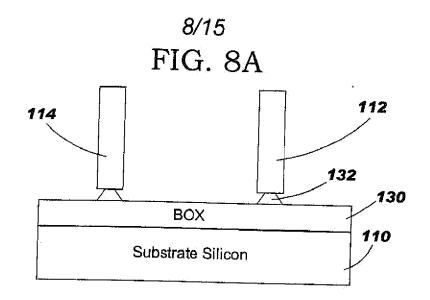
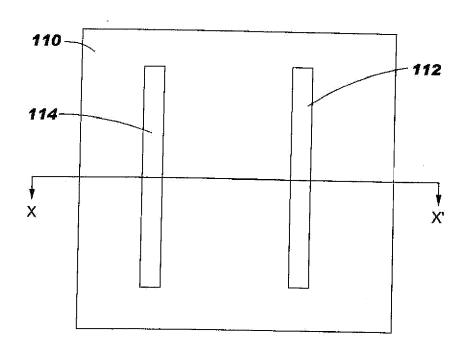


FIG. 8B



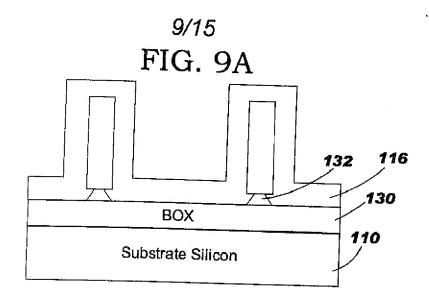
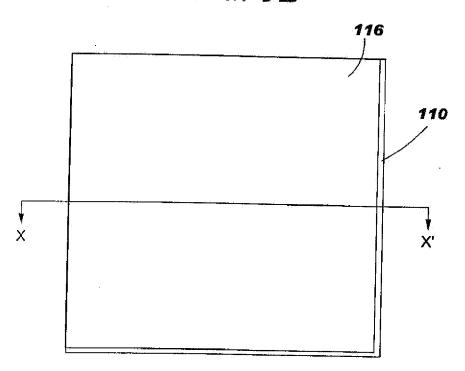


FIG. 9B



10/15 FIG. 10A

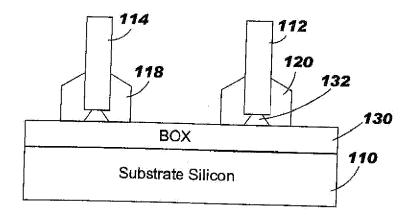
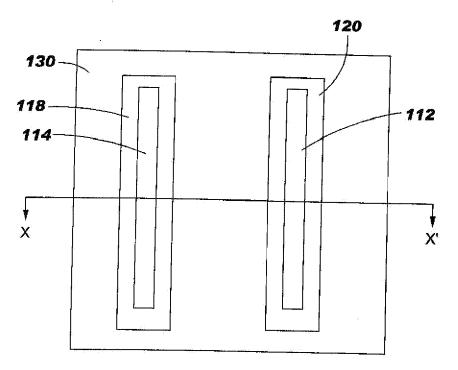


FIG. 10B



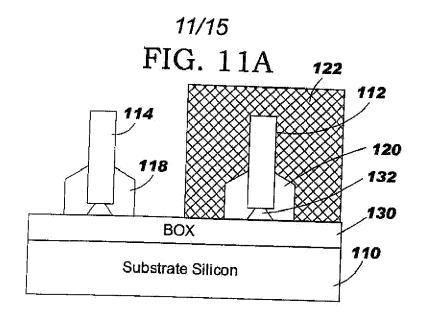
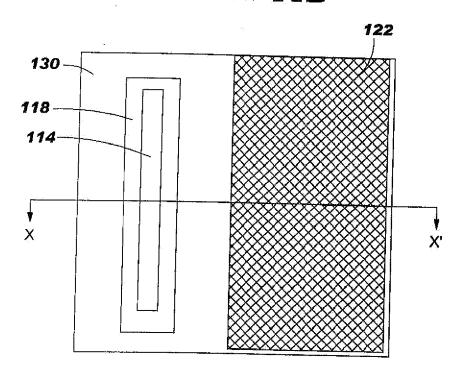


FIG. 11B



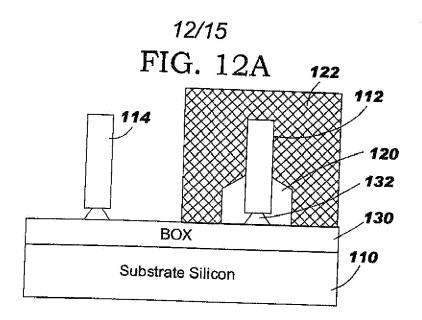
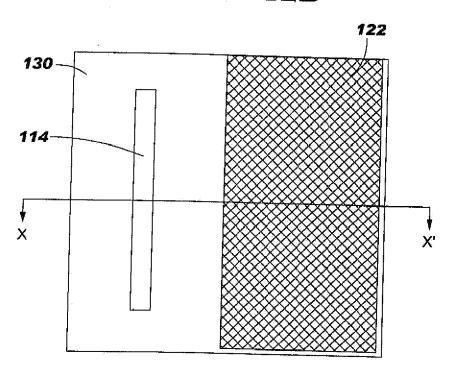


FIG. 12B



13/15 FIG. 13A

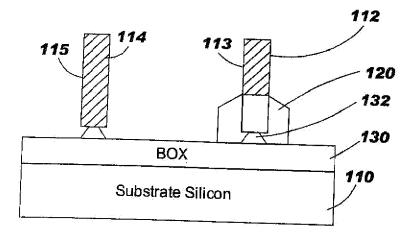
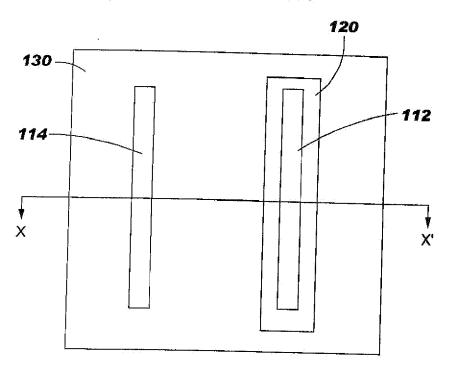


FIG. 13B



*14/15* FIG. 14A

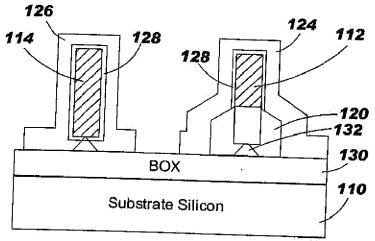
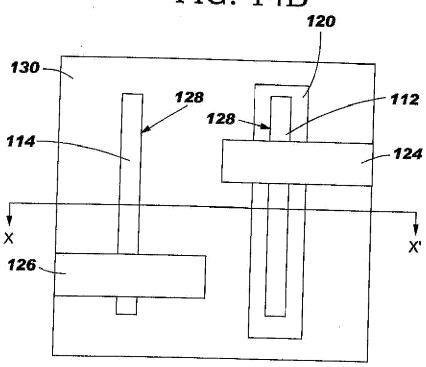


FIG. 14B



15/15 FIG. 15

